**Source Code:**

module prjctr(state,reset,grn,ylw,rd,an);

input[1:0] state;

input reset;

output reg [3:0]grn,ylw,rd;

output reg [3:0]an;

always@(reset or state)

begin

if(reset==0)

begin

grn=4'b0000;

//ylw=4'b0000;

ylw=4'b1111;

rd=4'b1111;

end

else

case (state)

2'b00:

begin

grn=4'b0001;

//ylw=4'b0010;

ylw=4'b1101;

rd=4'b1100;

end

2'b01:

begin

grn=4'b0010;

//ylw=4'b0100;

ylw=4'b1011;

rd=4'b1001;

end

2'b10:

begin

grn=4'b0100;

//ylw=4'b1000;

ylw=4'b0111;

rd=4'b0011;

end

default:

begin

grn=4'b1000;

//ylw=4'b0001;

ylw=4'b1110;

rd=4'b0110;

end

endcase

an=4'b1110;

end

endmodule

**Test bench :**

module tb;

// Inputs

reg [1:0] state;

reg reset;

// Outputs

wire [4:1] grn;

wire [4:1] ylw;

wire [4:1] rd;

// Instantiate the Unit Under Test (UUT)

prjctr uut (

.state(state),

.reset(reset),

.grn(grn),

.ylw(ylw),

.rd(rd)

);

initial begin

// Initialize Inputs

state = 2'b00;

reset = 1;

// Wait 100 ns for global reset to finish

#100;

state = 2'b01;

reset = 0;

// Wait 100 ns for global reset to finish

#100;

state = 2'b01;

reset = 1;

// Wait 100 ns for global reset to finish

#100;

state = 2'b10;

reset = 1;

// Wait 100 ns for global reset to finish

#100;

state = 2'b11;

reset = 1;

// Wait 100 ns for global reset to finish

#100;

state = 2'b00;

reset = 1;

// Wait 100 ns for global reset to finish

#100;

state = 2'b01;

reset = 1;

// Wait 100 ns for global reset to finish

#100;

state = 2'b10;

reset = 1;

// Wait 100 ns for global reset to finish

#100;

state = 2'b11;

reset = 1;

// Wait 100 ns for global reset to finish

#100;

state = 2'b00;

reset = 1;

// Wait 100 ns for global reset to finish

#100;

end

endmodule

UCF FILE:

net "reset" loc=p11;

net "state[0]" loc=l3;

net "state[1]" loc=k3;

net "grn[0]" loc=m5;

net "grn[1]" loc=m11;

net "grn[2]" loc=p7;

net "grn[3]" loc=p6;

net "rd[0]" loc=n5;

net "rd[1]" loc=n4;

net "rd[2]" loc=p4;

net "rd[3]" loc=g1;

net "an[0]" loc=f12;

net "an[1]" loc=m13;

net "an[2]" loc=j12;

net "an[3]" loc=k14;

net "ylw[0]" loc=l13;

net "ylw[1]" loc=l14;

net "ylw[2]" loc=m12;

net "ylw[3]" loc=p12;